Analog Power

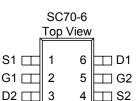
N-Channel 60-V (D-S) MOSFET

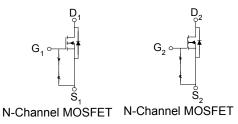
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe S1 SC70-6 saves board space G1 □□
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)}(\Omega)$ $I_D(A)$		
60	$2.0 @ V_{GS} = 4.5V$	0.32	
	$3.0 @ V_{GS} = 2.5V$	0.26	





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	20	v	
	$T_A=25^{\circ}C$	-I _D	0.32		
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$		0.26	А	
Pulsed Drain Current ^b		I _{DM}	0.7		
Continuous Source Current (Diode Conduction) ^a		I _S	0.25	А	
	$T_A=25^{\circ}C$	P _D	0.3	W	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	I D	0.21	٧V	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	t <= 5 sec	D	415	°C/W
	Steady-State	K _{THJA}	460	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Skal	Test Conditions	Limits			Unit
	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1.0			V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±10	uA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 48 V, V_{GS} = 0 V$			1	uA
Zero Gate Voltage Drain Current	¹ DSS	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			50	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	0.3			Α
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 0.3 \text{ A}$			2	Ω
Dram-Source On-Resistance		$V_{GS} = 4.5 \text{ V}, I_D = 0.2 \text{ A}$			3	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 4.5 \text{ V}, I_D = 0.3 \text{ A}$		8		S
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 0.2$ A, $V_{\rm GS} = 0$ V		1.10		V
Dynamic ^b						
Total Gate Charge	Qg			0.4		
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 V, V_{GS} = 5 V, I_D = 0.3 A$		0.1		nC
Gate-Drain Charge	Q _{gd}			0.1		
Turn-On Delay Time	t _{d(on)}			10		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 30 \Omega, I_D = 0.3 \text{ A},$ $V_{GEN} = 10 \text{ V}$		6		ns
Turn-Off Delay Time	t _{d(off)}			20		
Fall-Time	t _f			3		

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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